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10/820,058	04/08/2004	Takehiro Suzuki	1035-505	7339

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EXAMINER	
DOAN, THERESA T	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,058	SUZUKI, TAKEHIRO	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The RCE and the amendment filed 12/28/06 has being acknowledged and entered. By this amendment claims 1-13 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 6-7 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Saito et al. (U.S. Pat. 6,731,007).

Regarding claim 1, Saito (Fig. 60) discloses a semiconductor device, comprising: a semiconductor substrate 1 having formed thereon a semiconductor element (FET with 3n/3p); a first wiring layer 21C formed on said semiconductor substrate 1 above an operating region (3nd) where said semiconductor element is formed, said first wiring layer 21C being electrically connected to said operating region 3nd; a second wiring layer 13L formed on said semiconductor substrate 1 above said first wiring layer 21C; and a bonding pad 102 to be electrically connected to an external connection terminal, formed on said semiconductor substrate 1 above said second wiring layer 13L, at least

a part of said bonding pad 102 being located above said operating region 3nd, wherein said second wiring layer 13L includes a plurality of wirings formed in the region under said bonding pad 102, a predetermined wiring 13L (on left side) of said plurality of wirings is electrically connected to said bonding pad 102, and an insulating film 15 is provided for insulating said bonding pad 102 from other wirings 13L (on right side) than the predetermined wiring among said plurality of wirings, so that a plurality of wirings of the second wiring layer 13L, which are located directly under the bonding pad 102 are insulated from the bonding pad 102 by the insulating film 15, wherein said insulating film 15 is formed over said other wirings 13L so as to directly contact the bonding pad 316; said other wirings 13L provided parallel to the edges of said bonding pad 102 are not formed in regions right under the edges (see Fig. 60), and wherein at least one of said other wirings 13L of said second wiring layer that is insulated from said bonding pad 102 is electrically connected to the first wiring layer 21C by way of a via 20C defined in an insulator 4d located between said first and second wirings layers (21C,13L); and said insulating film 15 is made up of an inorganic insulating film only so that no organic insulating film is provided between the other wiring 13L and the bonding pad 102 (col. 18, lines 14-20).

Regarding claim 6, Saito (Fig. 60) discloses the semiconductor device wherein the bonding pad 102 is to be electrically connected to an inner lead by an inner lead bonding process. The bonding pad of Saito is capable of electrically connected "to an inner lead by an inner lead. It is note that the process limitation "by an inner lead

bonding process" would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985). In addition "to be electrically connected to an inner lead" does not define any distinct structure.

Regarding claim 7, Saito (Fig. 60) discloses a semiconductor device, comprising: a semiconductor substrate 1 having formed thereon a semiconductor element (FET with 3n/3p); a first wiring layer 21C formed on said semiconductor substrate 1 above an operating region (3nd) where said semiconductor element is formed, said first wiring layer 21C being electrically connected to said operating region 3nd; a second wiring layer 13L formed on said semiconductor substrate 1 above said first wiring layer 21C; and a bonding pad 102 to be electrically connected to an inner lead, formed on said semiconductor substrate 1 above said second wiring layer 13L, at least a part of said bonding pad 102 being located above said operating region 3nd, wherein said second wiring layer 13L includes a plurality of wirings formed in the region under said bonding pad 102, a predetermined wiring 13L (on left side) of said plurality of wirings is electrically connected to said bonding pad 102, and an insulating film 15 is provided for insulating said bonding pad 102 from other wirings 13L (on right side) than the predetermined wiring among said plurality of wirings, so that a plurality of wirings of the second wiring layer 13L, which are located directly under the bonding pad 102 are insulated from the bonding pad 102 by the insulating film 15, wherein said insulating film 15 is formed over said other wirings 13L so as to directly contact the bonding pad 316;

said other wirings 13L provided parallel to the edges of said bonding pad 102 are not formed in regions right under the edges of the regions electrically connected to the inner lead on the surface of the bonding pad 102 (see Fig. 60), and wherein at least one of said other wirings 13L of said second wiring layer that is insulated from said bonding pad 102 is electrically connected to the first wiring layer 21C by way of a via 20C defined in an insulator 4d located between said first and second wirings layers (21C,13L); and said insulating film 15 is made up of an inorganic insulating film only so that no organic insulating film is provided between the other wiring 13L and the bonding pad 102 (col. 18, lines 14-20). It is note that the process limitation "by an inner lead bonding process" would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985). In addition "to be electrically connected to an inner lead" does not define any distinct structure.

Regarding claim 10, Saito discloses the semiconductor device wherein said insulating film 15 is made up of a silicone oxide film and a silicone nitride film (col. 18, lines 14-20). It is note that the process limitation "formed by CVD" would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-5, 8-9, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (U.S. Pat. 6,731,007) in view of Applicant Admitted Prior Art (APA).

Regarding claims 2-3, 8-9, Saito does not discloses the in expanded regions right under said expanded regions as expanded with a stress in a process of electrically connecting said bonding pad to an external connection terminal, wherein respective lengths of the expanded regions in the expanding direction of said bonding pad are set to fall in a range of from 2 micron to 3 micron.

However, APA discloses (Fig. 9) a semiconductor device comprises a wire 202 having bonding pad 201, an expanded regions right under said expanded regions 201a-b as expanded with a stress in a process of electrically connecting said bonding pad to an external connection terminal 208, wherein respective lengths of the expanded regions in the expanding direction of said bonding pad 201 are set to fall in a range of from 2 micron (see background of the invention in fig. 9). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to conclude that the bonding pad 102 of Saito would have the expanded regions as claimed. Where the claimed and the prior art products are identical or substantially

identical in structure or composition, or are produced by identical or substantially identical processes, a prima facie case of either anticipation or obviousness has been established. In re Best, 195 USPQ 430,433 (CCPA 1977).

Regarding claims 4-5, Saito does not disclose the semiconductor device wherein said bonding pad 102 and said external connection terminal are electrically connected by the chip-on-glass or chip-on board.

However, APA discloses the semiconductor device wherein bonding pad 201 and said external connection terminal are electrically connected by the chip-on-glass (COG) or TCP (see background of the invention). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the teaching of APA with Saito for intended use because the recitation "chip-on-glass" or "chip-on-board" of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

Regarding claim 11, Saito (Fig. 60) discloses a semiconductor device, comprising: a semiconductor substrate 1 having formed thereon a semiconductor element (FET with 3n/3p); a first wiring layer 21C formed on said semiconductor substrate 1 above an operating region (3nd) where said semiconductor element is formed, said first wiring layer 21C being electrically connected to said operating region 3nd; a second wiring layer 13L formed on said semiconductor substrate 1 above said

first wiring layer 21C; and a bonding pad 102 to be electrically connected to an external connection terminal, formed on said semiconductor substrate 1 above said second wiring layer 13L, at least a part of said bonding pad 102 being located above said operating region 3nd, wherein said second wiring layer 13L includes a plurality of wirings, a predetermined wiring 13L (on left side) of said plurality of wirings is electrically connected to said bonding pad 102, and an insulating film 15 is provided for insulating said bonding pad 102 from other wirings 13L (on right side) than the predetermined wiring among said plurality of wirings, so that a plurality of wirings of the second wiring layer 13L, which are located directly under the bonding pad 102 are insulated from the bonding pad 102 by the insulating film 15, wherein said insulating film 15 is formed over said other wirings 13L so as to directly contact the bonding pad 316; said other wirings 13L provided parallel to the edges of said bonding pad 102 are not formed in regions right under the edges (see Fig. 60), and wherein at least one of said other wirings 13L of said second wiring layer that is insulated from said bonding pad 102 is electrically connected to the first wiring layer 21C by way of a via 20C defined in an insulator 4d located between said first and second wirings layers (21C,13L); and said insulating film 15 is made up of an inorganic insulating film only so that no organic insulating film is provided between the other wiring 13L and the bonding pad 102 (col. 18, lines 14-20).

Saito does not expressly disclose under the edges in the lengthwise direction of bonding pad to 3 micron outside the region. It would have been obvious to one of ordinary skill in art to use the general distance teaching of Saito in the range as claimed, because it has been held that where the general conditions of the claims are discloses

in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233,235 (CCPA 1955). In this case, there is nothing in the present application to indicate that the claimed under the edges in the lengthwise direction of bonding pad to 3 micron outside the region is critical. Therefore, the forming under the edges in the lengthwise direction of bonding pad to 3 micron outside the region can be optimized during experimentation depending upon operating the device in a particular application.

Regarding claim 12, Saito discloses the semiconductor device wherein said insulating film 15 is made up of an inorganic insulating film only.

Regarding claim 13, Saito discloses the semiconductor device wherein at least a part of said other wirings 13L is formed in a region right under said bonding pad 102, and other wirings formed in the region right under the bonding pad 102 are formed only in a region right under a region electrically connected to an inner lead on a surface of said bonding pad 102 (Fig. 60).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 6, 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lien (U.S. 5,989,991) in view of Izumitani et al. (U.S. 6,727,590).

Regarding claim 1, Lien (Fig. 6) discloses a semiconductor device, comprising: a semiconductor substrate 201 having formed thereon a semiconductor element (FET with 202/205/203); a first wiring layer 210 formed on said semiconductor substrate 201 above an operating region 202 where said semiconductor element is formed, said first wiring layer 210 being electrically connected to said operating region 202; a second wiring layer 311 formed on said semiconductor substrate 201 above said first wiring layer 210; and a bonding pad 316 to be electrically connected to an external connection terminal, formed on said semiconductor substrate 201 above said second wiring layer 311, at least a part of said bonding pad 316 being located above said operating region 202, wherein said second wiring layer 311 includes a plurality of wirings 324-326 formed in the region under said bonding pad 316, a predetermined wiring (portion in contact 311 and 210 layers) of said plurality of wirings is electrically connected to said bonding pad 316, and an insulating film 308 is provided for insulating said bonding pad 316 from other wirings 324-326 than the predetermined wiring among said plurality of wirings, so that a plurality of wirings 324-326 of the second wiring layer 311, which are located directly under the bonding pad are insulated from the bonding pad 316 by the insulating film 308, wherein said insulating film 308 is formed over said other wirings 324-326 so as to directly contact the bonding pad 316; said other wirings 324-326 provided parallel to the edges of said bonding pad 316 are not formed in regions right under the edges (see Fig. 6); and said insulating film 308 is made up of an inorganic insulating film only

so that no organic insulating film is provided between the other wiring 324-326 and the bonding pad 316.

Lien does not disclose at least one of said other wirings of said second wiring layer that is insulated from said bonding pad is electrically connected to the first wiring layer by way of a via defined in an insulator located between said first and second wirings layers.

However, Izumitani (Fig. 36) teaches at least one of said other wirings of said second wiring layer 158 that is insulated from said bonding pad 171 is electrically connected to the first wiring layer 154 by way of a via defined in an insulator 155 located between said first and second wirings layers (154,158) in order to provide electrical connect between the first and the second wiring layers (column 5, lines 42-45). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device of Lien by forming the second wiring layer is electrically connected to the first wiring layer 154 by way of a via in order to provide electrically connect between the first and the second wiring layers, as taught by Izumitani (column 5, lines 42-45).

Regarding claim 6, Lien discloses the semiconductor device wherein the bonding pad 316 is to be electrically connected to an inner lead by an inner lead bonding process.

The bonding pad of Lien is capable of electrically connected "to an inner lead by an inner lead. The limitation "by an inner lead bonding process" does not carry weight in

a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985). In addition "to be electrically connected to an inner lead" does not define any distinct structure.

Regarding claim 7, Lien (Fig. 6) discloses a semiconductor device, comprising: a semiconductor substrate 201 having formed thereon a semiconductor element (FET with gate and S/D); a first wiring layer 210 formed on said semiconductor substrate 201 at above an operating region 202 where said semiconductor element is formed, said first wiring layer 210 being electrically connected to said operating region 202; a second wiring layer 311 formed on said semiconductor substrate 210 at above said first wiring layer 210; and a bonding pad 316 to be electrically connected to an inner lead 317, formed on said semiconductor substrate 201 at above said second wiring layer 311, at least a part of said bonding pad 316 being located right above said operating region 202, wherein said second wiring layer 311 includes a plurality of wirings 324-326 formed in the region right under said bonding pad 316, a predetermined wiring (portion in contact with 311 and 210) of said plurality of wirings is connected to said bonding pad 316, and an insulating film 308 is provided for insulating said bonding pad 316 from other wirings 324-326 than the predetermined wiring among said plurality of wirings so that a plurality of wirings of the second wiring layer, which are located directly under the bonding pad are insulated from the bonding pad 316 by the insulating film 308, and wherein said insulating film 308 is formed over other wirings so as to directly contact the bonding pad 316; said other wirings 324-326 provided parallel to edges of said bonding pad 316 are not formed in regions right under the edges of the regions electrically

connected to the inner lead on the surface of said bonding pad 316; and said insulating film 308 comprises an inorganic insulating film only, so that a bottom surface of the bonding pad 316 does not contact any organic insulating film.

Lien does not disclose at least one of said other wirings of said second wiring layer that is insulated from said bonding pad is electrically connected to the first wiring layer by way of a via defined in an insulator located between said first and second wirings layers.

However, Izumitani (Fig. 36) teaches at least one of said other wirings of said second wiring layer 158 that is insulated from said bonding pad 171 is electrically connected to the first wiring layer 154 by way of a via defined in an insulator 155 located between said first and second wirings layers (154,158) in order to provide electrical connect between the first and the second wiring layers (column 5, lines 42-45). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device of Lien by forming the second wiring layer is electrically connected to the first wiring layer 154 by way of a via in order to provide electrically connect between the first and the second wiring layers, as taught by Izumitani (column 5, lines 42-45).

Regarding claim 10, Lien discloses the semiconductor device wherein said insulating film 308 is made up of a silicone oxide film and a silicone nitride film. The limitation "formed by CVD" would not carry patentable weight in this claim drawn to a structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

8. Claims 2-5, 8-9, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lien (U.S. 5,989,991) in view of Izumitani et al. (U.S. 6,727,590) and further in view of Applicant Admitted Prior Art (APA).

Regarding claims 2-3, 8-9, Lien does not expressly discloses the in expanded regions right under said expanded regions as expanded with a stress in a process of electrically connecting said bonding pad to an external connection terminal, wherein respective lengths of the expanded regions in the expanding direction of said bonding pad are set to fall in a range of from 2 micron to 3 micron.

However, APA discloses (Fig. 9) a semiconductor device comprises a wire 202 having bonding pad 201, an expanded regions right under said expanded regions 201a-b as expanded with a stress in a process of electrically connecting said bonding pad to an external connection terminal 208, wherein respective lengths of the expanded regions in the expanding direction of said bonding pad 201 are set to fall in a range of from 2 micron (see background of the invention in fig. 9). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to conclude that the bonding pad 316 of Lien would have the expanded regions as claimed. Where the claimed and the prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a prima facie case of either anticipation or obviousness has been established. In re Best, 195 USPQ 430,433 (CCPA 1977).

Regarding claims 4-5, Lien does not disclose the semiconductor device wherein said bonding pad 316 and said external connection terminal are electrically connected by the chip-on-glass or chip-on board.

However, APA discloses the semiconductor device wherein bonding pad 201 and said external connection terminal are electrically connected by the chip-on-glass (COG) or TCP (see background of the invention). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the teaching of APA with Lien for intended use because the recitation "chip-on-glass" or "chip-on-board" of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

Regarding claim 11, Lien discloses (Fig. 6) a semiconductor device, comprising: a semiconductor substrate 201 having formed thereon a semiconductor element (FET with gate and S/D); a first wiring layer 210 formed on said semiconductor substrate 201 at above an operating region 202 where said semiconductor element is formed, said first wiring layer 210 being electrically connected to said operating region 202; a second wiring layer 311 formed on said semiconductor substrate 201 at above said first wiring layer 210; and a bonding pad 316 to be electrically connected to an external connection terminal (Fig. 6), formed on said semiconductor substrate 201 at above said second wiring layer 311, at least a part of said bonding pad 316 being located right above said operating region 202, wherein said second wiring layer 311 includes a

plurality of wirings 324-326, a predetermined wiring (portion in contact with 311 and 210) of said plurality of wirings is connected to said bonding pad 316, and an insulating film 308 is provided for insulating said bonding pad 316 from other wirings than the predetermined wiring among said plurality of wirings so that a plurality of wirings of the second wiring layer, which are located directly under the bonding pad are insulated from the bonding pad 316 by the insulating film 308, and wherein said insulating film is formed above said other wirings so as directly contact the bonding pad 316; said other wirings 324-326 are formed so as to avoid regions right under the edges in the lengthwise direction of said bonding pad 316 and said insulating film 308 includes an inorganic insulating film, so that no organic insulating film 308 is provided between the other wiring and the bonding pad 316 (Fig. 6).

Lien does not disclose at least one of said other wirings of said second wiring layer that is insulated from said bonding pad is electrically connected to the first wiring layer by way of a via defined in an insulator located between said first and second wirings layers.

However, Izumitani (Fig. 36) teaches at least one of said other wirings of said second wiring layer 158 that is insulated from said bonding pad 171 is electrically connected to the first wiring layer 154 by way of a via defined in an insulator 155 located between said first and second wirings layers (154,158) in order to provide electrical connect between the first and the second wiring layers (column 5, lines 42-45). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device of Lien by forming the second

wiring layer is electrically connected to the first wiring layer 154 by way of a via in order to provide electrically connect between the first and the second wiring layers, as taught by Izumitani (column 5, lines 42-45).

Lien does not expressly disclose under the edges in the lengthwise direction of bonding pad to 3 micron outside the region.

However, Lien clearly discloses a lateral distance in the range of 7 to 8 micron (col. 5, line 65), and general distance from the edge of the bonding pad 316 to the second wire layer. Accordingly, it would have been obvious to one of ordinary skill in art to use the general distance teaching of Lien in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233,235 (CCPA 1955). In this case, there is nothing in the present application to indicate that the claimed under the edges in the lengthwise direction of bonding pad to 3 micron outside the region is critical. Therefore, the forming under the edges in the lengthwise direction of bonding pad to 3 micron outside the region can be optimized during experimentation depending upon operating the device in a particular application.

Regarding claim 12, Lien discloses the semiconductor device wherein said insulating film 308 is made up of an inorganic insulating film only.

Regarding claim 13, Lien discloses the semiconductor device wherein at least a part of said other wirings 324-326 is formed in a region right under said bonding pad 316, and other wirings formed in the region right under the bonding pad 316 are formed only in a region right under a region electrically connected to an inner lead 317 on a surface of said bonding pad 316 (Fig. 6).

Response to Arguments

9. Applicant's arguments filed on 12/28/06 have been fully considered but are moot in view of the new ground(s) of rejection.

The Applicant's arguments, addressed to the amended claims are considered in the rejections shown above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

T.D.
March 18, 2007.

THERESA DOAN
PRIMARY PATENT EXAMINER